Listing of the Claims:

Claims 1-17. (Cancelled).

Claim 18. (Currently Amended) An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line;

a plurality of common electrodes extending perpendicular to the common line, the plurality of common electrodes being divided into first and second portions of respective first and second domains;

a plurality of pixel electrodes arranged alternately with the plurality of common electrodes, the plurality of pixel electrodes being divided into first and second portions of the respective first and second domains;

an auxiliary common electrode perpendicularly contacting each of the common electrodes; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes;

wherein the auxiliary pixel ~~electrodes~~ electrode is spaced apart from the auxiliary common electrode; and the pixel ~~electrodes are~~ electrode is on a same layer as the auxiliary pixel electrode.

Claim 19. (Currently Amended) An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line, the common line including first and second auxiliary common lines perpendicular to the common line;

a plurality of common electrodes extending perpendicular to the first and second auxiliary common lines, the plurality of common electrodes being divided into first and second portions of respective first and second domains;

a plurality of pixel electrodes arranged alternately with the plurality of common electrodes, the plurality of pixel electrodes being divided into first and second portions of the respective first and second domains;

an auxiliary common electrode perpendicularly contacting each of the common electrodes; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes, wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode.

Claim 20. (Currently Amended) An array substrate for an IPS-LCD device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line, the common line including a plurality of common electrodes extending perpendicular to the common line;

a plurality of pixel electrodes arranged alternately with the plurality of common electrodes; and

a plurality of auxiliary electrodes connecting the plurality of common and pixel electrodes [[in]] to form a multi-domain having a check pattern.

Claims 21-29. (Cancelled)

Claim 30. (Currently Amended) An array substrate for an LCD-device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a pixel region surrounded by the gate and data lines, the pixel region including first and second domains;

transverse pixel and common electrodes disposed on the first domain and parallel to the gate line, the transverse pixel and common electrodes being alternately arranged;

perpendicular pixel and common electrodes disposed on the second domain and perpendicular to the transverse pixel and common electrodes, respectively, the perpendicular pixel and common electrodes being alternately arranged; and

an alignment layer having first and second rubbing directions, the first and second rubbing directions corresponding to the first and second domains, respectively,

wherein the first and second rubbing directions are symmetrical with respect to a line parallel to the gate line.

Claim 31. (Cancelled)

Claim 32. (Cancelled)

Claim 33. (Currently Amended) An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a gate insulating layer over the gate line;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a first passivation layer over the gate insulating layer, the data line and thin film transistor;

a plurality of pixel electrodes on the first passivation layer, the plurality of pixel electrodes being divided into first and second portions of respective first and second domains;

a second passivation layer over the pixel electrodes;

a common line on the second passivation layer and parallel to the gate line, the common line including first and second auxiliary common lines perpendicular to the common line;

a plurality of common electrodes extending perpendicular to the first and second auxiliary common lines, the plurality of common electrodes being divided into first and second portions of the respective first and second domains;

an auxiliary common electrode perpendicularly contacting each common electrode; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes;

wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode; and

wherein the pixel electrodes are arranged alternately with the common electrodes.

34. (Currently Amended) An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a gate insulating layer on the gate line;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a first passivation layer over the gate insulating layer, the data line and the thin film transistor;

a plurality of pixel electrodes on the first passivation layer, the plurality of pixel electrodes being divided into first and second portions of respective first and second domains;

a second passivation layer over the pixel electrodes;

a common line on the second ~~pass~~ passivation layer parallel to the gate line;

a plurality of common electrodes on the second passivation layer perpendicular to the common line and arranged alternatively with the pixel electrodes, the plurality of common electrodes being divided into first and second portions of the respective first and second domains;

~~a plurality of common electrodes on the second passivation layer perpendicular to the common line and arranged alternatively with the pixel electrodes;~~

an auxiliary common electrode perpendicularly contacting each of the common electrodes; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes;

wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode.

AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to FIGs. 1-7 to delete "related art" and replace with "prior art" in the legend. Replacement sheets have been provided for the entire set of drawings, FIGS. 1-27B.

Attachment: Replacement sheets
Annotated sheets showing changes